AMENDMENTS TO THE CLAIMS

By this Response, Applicant is amending Claims 1–3, 7, 9, 11–13, 15, 19–21, 34, 35, 37, 45, 46, 48 and 53 and is cancelling Claims 8, 14, 18, 30, 31, 41 and 51 without prejudice or disclaimer. Claims 4–6, 10, 16, 17, 22–29, 32, 33, 36, 38–40, 42–44, 47, 49, 50 and 52 remain as originally filed, and new Claim 54 has been added.

1. (Currently Amended) A method of making a microprocessing system comprising:

coupling a data cache having a plurality of cache lines to a string execution unit;

coupling a bus interface unit to the string execution unit;

coupling a general execution unit to the bus interface unit; and

coupling a barrel shifter to said data cache so as to shift an entire cache line of the plurality of cache lines a selected number of bytes in a single processor cycle.

2. (Currently Amended) The method of Claim 1, additionally comprising coupling a plurality of comparators to said data cache so as to compare data in [[an]] the entire cache line to a test data string in a single processor cycle.

3. (Currently Amended) The method of Claim 1, additionally comprising coupling a plurality of subtractors to said data cache so as to compare data in [[an]] the entire cache line to a test data string in a single processor cycle.

4. (Original) The method of Claim 1, wherein the string execution unit is in association with a memory controller.

5. (Original) The method of Claim 4, additionally comprising coupling a main memory to the memory controller.

6. (Original) The method of Claim 5, wherein the main memory comprises a DRAM circuit.

7. (Currently Amended) The method of Claim 1, additionally comprising coupling a register to the barrel shifter so as to store data shifted out of the entire cache line by the barrel shifter.

8. (Cancelled)

9. (Currently Amended) The method of Claim 1 [[8]], ~~additionally comprising coupling a general execution unit to the bus interface unit,~~ wherein the general execution unit is configured to perform arithmetic and logical instructions on data.

10. (Original) The method of Claim 1, wherein the data cache is a Level 1 cache.

11. (Currently Amended) A processor for data string manipulation, the processor comprising:

a data cache comprising a plurality of cache lines;

a string execution unit coupled to said data cache;

a memory controller coupled to the string execution unit;

a general execution unit coupled to the memory controller; and

a barrel shifter coupled to said data cache, said barrel shifter configured so as to shift an entire cache line of the plurality of cache lines a selected number of bytes in a single processor cycle.

12. (Currently Amended) The processor of Claim 11, further comprising a plurality of comparators coupled to the data cache so as to compare data in [[an]] the entire cache line to a test data string in a single processor cycle.

13. (Currently Amended) The processor of Claim 11, further comprising a plurality of subtractors coupled to the data cache so as to compare data in [[an]] the entire cache line to a test data string in a single processor cycle.

14. (Cancelled)

15. (Currently Amended) The processor of Claim 11 [[14]], further comprising a main memory coupled to the memory controller.

16. (Original) The processor of Claim 15, wherein the main memory comprises a DRAM circuit.

17. (Original) The processor of Claim 11, wherein the execution unit is in association with a bus interface unit.

18. (Cancelled)

19. (Currently Amended) The processor of Claim 11 [[18]], wherein said memory controller is configured to be alternatively and independently controlled by the string execution unit and the general execution unit.

20. (Currently Amended) The processor of Claim 11, further comprising a register coupled to the barrel shifter, the register configured to store data shifted out of the entire cache line by the barrel shifter.

21. (Currently Amended) A method of making a processor, the method comprising:

coupling a data cache to a first execution unit, wherein the first execution unit is in association with a bus interface unit;

coupling a second execution unit to the bus interface unit; and

coupling a cache line shifter to the data cache so as to shift a cache line a selected number of bytes.

22. (Original) The method of Claim 21, additionally comprising coupling a plurality of comparators to the data cache.

23. (Original) The method of Claim 21, additionally comprising coupling a plurality of subtractors to the data cache.

24. (Original) The method of Claim 21, wherein the cache line shifter comprises a barrel shifter.

25. (Original) The method of Claim 21, wherein the cache line shifter is configured to shift an entire cache line in a single processor cycle.

26. (Original) The method of Claim 21, wherein said data cache comprises a Level 1 cache.

27. (Original) The method of Claim 21, wherein said data cache comprises a Level 2 cache.

28. (Original) The method of Claim 21, additionally comprising coupling a memory controller to the first execution unit

29. (Original) The method of Claim 28, additionally comprising coupling a main memory to the memory controller.

30. (Cancelled)

31. (Cancelled)

32. (Original) The method of Claim 21 [[31]], wherein the first execution unit is configured to perform assembly language string manipulation instructions and the second execution unit is configured to perform assembly language arithmetic and logic instructions.

33. (Original) The method of Claim 21, additionally comprising coupling a register to the cache line shifter so as to store data shifted out of the cache line by the cache line shifter.

34. (Currently Amended) A processor comprising:

a data cache configured to hold at least one cache line;

a string execution unit coupled to the data cache;

a bus interface unit coupled to the string execution unit;

a second execution unit coupled to the bus interface unit; and

a cache line shifter coupled to the data cache so as to shift a first cache line of the at least one cache line a selected number of bytes.

35. (Currently Amended) The processor of Claim 34, further comprising a plurality of comparators coupled to said data cache, said comparators configured to compare data in [[an]] the entire first cache line to a test data string in a single processor cycle.

36. (Original) The processor of Claim 34, wherein the cache line shifter comprises a barrel shifter.

37. (Currently Amended) The processor of Claim 34, wherein the cache line shifter is configured to shift ~~an entire~~ the first cache line in a single processor cycle.

38. (Original) The processor of Claim 34, wherein said data cache comprises a Level 1 cache.

39. (Original) The processor of Claim 34, further comprising a memory controller coupled to the string execution unit.

40. (Original) The processor of Claim 34, further comprising a main memory coupled to the memory controller.

41. (Cancelled)

42. (Original) The processor of Claim 34, further comprising a register coupled to the cache line shifter so as to store data shifted out of the cache line by the cache line shifter.

43. (Original) The processor of Claim 35, further comprising a decoder coupled to the plurality of comparators so as to identify a portion of the cache line that contains data matching at least a portion of the test data string.

44. (Original) The processor of Claim 43, wherein the decoder is coupled to the string execution unit and is configured to forward a cache address of the matching cache line data to the string execution unit.

45. (Currently Amended) A processor for data string manipulation, the processor comprising:

a data cache means for storing a plurality of cache lines comprising a plurality of bytes of data;

a string execution means for manipulating the data in the data cache means, the string execution means coupled to said data cache means;

a general execution means for performing arithmetic and logical instructions;

a bus interface means coupled to the string execution means and to the general execution means; and

a means for shifting [[the]] a selected cache line of the plurality of cache lines.

46. (Currently Amended) The processor of Claim 45, further comprising a means for comparing the selected cache line with a test data in a single processor cycle so as to detect a matching portion of the selected cache line.

47. (Original) The processor of Claim 46, wherein the means for comparing comprises a plurality of comparators.

48. (Currently Amended) The processor of Claim 47, wherein the number of the plurality of comparators is equal to the number of bytes in the selected cache line.

49. (Original) The processor of Claim 45, further comprising a memory controller in association with the string execution means.

50. (Original) The processor of Claim 49, further comprising a main memory coupled to the memory controller.

51. (Cancelled)

52. (Original) The processor of Claim 45, wherein the means for shifting comprises a barrel shifter.

53. (Currently Amended) The processor of Claim 45, further comprising a register coupled to the means for shifting so as to store data shifted out of the selected cache line by the means for shifting.

54. (New) A method of making a processor, the method comprising:

coupling a data cache to a first execution unit;

coupling a plurality of subtractors to the data cache; and

coupling a cache line shifter to the data cache so as to shift a cache line of the data cache a selected number of bytes.